IN THE CLAIMS:

The text of all pending claims, (including withdrawn claims) is set forth below. Cancelled and not entered claims are indicated with claim number and status only. The claims as listed below show added text with underlining and deleted text with ~~strikethrough~~. The status of each claim is indicated with one of (original), (currently amended), (cancelled), (withdrawn), (new), (previously presented), or (not entered).

Please AMEND claims 1 and 2 in accordance with the following:

1. (currently amended) A semiconductor package, provided with a multilayer interconnect structure, for mounting a semiconductor chip on its top surface, wherein:

a topmost stacked structure of the multilayer interconnect structure includes a capacitor structure, said capacitor structure having a dielectric layer comprised of a mixed electrodeposited layer of a high dielectric constant inorganic filler and an insulating resin and including chip connection pads for directly connecting top electrodes and bottom electrodes with electrodes of said semiconductor chip,

wherein the dielectric layer is selectively provided only on an electrode of the capacitor structure.

2. (currently amended) A semiconductor package, comprised of an insulating substrate on top and bottom surfaces of which multilayer interconnect structures are provided, for mounting a semiconductor chip on the top surface of a top surface multilayer interconnect structure, wherein:

the top surface multilayer structure includes a capacitor structure, said capacitor structure having a dielectric layer comprised of a mixed electrodeposited layer of a high dielectric constant inorganic filler and an insulating resin, and a topmost layer of said top surface multilayer interconnect structure includes chip connection pads for connecting top electrodes and bottom electrodes with electrodes of said semiconductor chip inside a region superposed with said capacitor structure in a plan view,

wherein the dielectric layer is selectively provided only on an electrode of the capacitor structure.

3. (previously presented) A semiconductor package as set forth in claim 2, wherein said top surface multilayer interconnect structure includes a plurality of stacked capacitor structures.

4. (previously presented) A semiconductor package as set forth in claim 1, wherein said inorganic filler is a powder of ceramic having a perovskite structure.

5. (previously presented) A semiconductor package as set forth in claim 1, wherein said insulating resin is a polyimide resin.

6. (previously presented) A semiconductor device comprised of a semiconductor package as set forth in claim 1 and a semiconductor chip directly connected at its electrodes to the chip connection pads.

7. (withdrawn) A method of production of a semiconductor package, provided with a multilayer interconnect structure, for mounting a semiconductor chip on its top surface, comprising:

a step of forming a capacitor structure in a topmost stacked structure of said multilayer interconnect structure,

said capacitor structure formation step comprising:

processing for forming at a bottommost layer of said topmost stacked structure a conductor layer for bottom electrodes of said capacitor structure,

processing for forming on said bottom electrodes by electrodeposition using an electrolyte comprised of high dielectric constant inorganic filler and insulating resin dispersed in a colloidal state a mixed electrodeposited layer of said inorganic filler and said insulating resin as a dielectric layer of said capacitor structure,

processing for forming on said dielectric layer a conductor layer for top electrodes of said capacitor structure, and

processing for forming inside said capacitor structure chip connection pads for directly connecting said top electrodes and said bottom electrodes with electrodes of said semiconductor chip.

8. (withdrawn) A method of production of a semiconductor package, comprised of an insulating substrate on top and bottom surfaces of which multilayer interconnect structures are provided, for mounting a semiconductor chip on the top surface of a top surface multilayer interconnect structure, comprising:

a step of forming a capacitor structure in a top surface multilayer interconnect structure,

said capacitor structure formation step comprising:

processing for forming a conductor layer for bottom electrodes of said capacitor

structure,

processing for forming on said bottom electrodes by electrodeposition using an electrolyte comprised of high dielectric constant inorganic filler and insulating resin dispersed in a colloidal state a mixed electrodeposited layer of said inorganic filler and said insulating resin as a dielectric layer of said capacitor structure,

processing for forming on said dielectric layer a conductor layer for top electrodes of said capacitor structure, and

processing for forming chip connection pads for connecting said top electrode and said bottom electrode with electrodes of said semiconductor chip in a region of the topmost layer of said top surface multilayer interconnect structure superposed with said capacitor layer in a plan view.

9. (withdrawn) A method of production of a semiconductor package as set forth in claim 8, further including a step of forming said capacitor structure by stacking a plurality of layers.

10. (previously presented) A semiconductor package as set forth in claim 2, wherein said inorganic filler is a powder of ceramic having a perovskite structure.

11. (previously presented) A semiconductor package as set forth in claim 3, wherein said inorganic filler is a powder of ceramic having a perovskite structure.

12. (previously presented) A semiconductor package as set forth in claim 2, wherein said insulating resin is a polyimide resin.

13. (previously presented) A semiconductor package as set forth in claim 3, wherein said insulating resin is a polyimide resin.

14. (previously presented) A semiconductor device comprised of a semiconductor package as set forth in claim 2 and a semiconductor chip directly connected at its electrodes to the chip connection pads.

15. (previously presented) A semiconductor device comprised of a semiconductor package as set forth in claim 3 and a semiconductor chip directly connected at its electrodes to the chip connection pads.